CLAIMS

What is Claimed is:

1. A semiconductor integrated circuit device comprising:

an external connection terminal;

an electrostatic discharge protection circuit connected to the external connection terminal;

a power supply line connected to the electrostatic discharge protection circuit;

a ground line connected to the electrostatic discharge protection circuit; and

an inter-power supply electrostatic discharge protection circuit that is connected to the power supply line and the ground line, and has a gate insulating element,

wherein the inter-power supply electrostatic discharge protection circuit comprises a first gate voltage control circuit capable of controlling the gate voltage of the gate insulating element.

2. The semiconductor integrated circuit device according to Claim 1,

wherein the gate insulating element is a first NMIS transistor whose source is connected to the ground line and whose drain is connected to the power supply line, and

wherein the first gate voltage control circuit comprises: a capacitor whose one end is connected to the power supply line and whose other end is connected to the gate of the first NMIS transistor; and a resistor whose one end is connected to the ground line and whose other end is connected to the gate of the first NMIS transistor.

3. The semiconductor integrated circuit device according to Claim 1,

wherein the gate insulating element is a first NMIS transistor whose source is

connected to the ground line and whose drain is connected to the power supply line, and

wherein the first gate voltage control circuit comprises: a first inverter section that is connected at its output to the gate of the first NMIS transistor, and has an uneven number of inverters; a resistor whose one end is connected to the power supply line and whose other end is connected to an input of the first inverter section; and a capacitor whose one end is connected to the ground line and whose other end is connected to the input of the first inverter section.

4. The semiconductor integrated circuit device according to Claim 1,

wherein the gate insulating element is a first NMIS transistor whose source is connected to the ground line and whose drain is connected to the power supply line, and

wherein the first gate voltage control circuit comprises: a first inverter section that is connected at its output to the gate of the first NMIS transistor, and has an even number of inverters; a resistor whose one end is connected to the ground line and whose other end is connected to an input of the first inverter section; and a capacitor whose one end is connected to the power supply line and whose other end is connected to the input of the first inverter section.

5. The semiconductor integrated circuit device according to Claim 1,

wherein the gate insulating element is a first NMIS transistor whose source is connected to the ground line and whose drain is connected to the power supply line, and

wherein the first gate voltage control circuit comprises: a first Schmidt trigger circuit connected at its output to the gate of the first NMIS transistor; a resistor whose one end is connected to the power supply line and whose other end is connected to an input of the first Schmidt trigger circuit; and a capacitor whose one end is connected to the ground line

and whose other end is connected to the input of the first Schmidt trigger circuit.

6. The semiconductor integrated circuit device according to Claim 1,

wherein the inter-power supply electrostatic discharge protection circuit further comprises:

a first PMIS transistor whose source is connected to the power supply line and whose drain is connected to the ground line; and

a second gate voltage control circuit capable of controlling the gate voltage of the first PMIS transistor.

7. The semiconductor integrated circuit device according to Claim 6,

wherein the second gate voltage control circuit comprises:

a resistor whose one end is connected to the power supply line and whose other end is connected to the gate of the first PMIS transistor; and

a capacitor whose one end is connected to the ground line and whose other end is connected to the gate of the first PMIS transistor.

8. The semiconductor integrated circuit device according to Claim 6,

wherein the second gate voltage control circuit comprises: a second inverter section that is connected at its output to the gate of the first PMIS transistor, and has an uneven number of inverters; a capacitor whose one end is connected to the power supply line and whose other end is connected to an input of the second inverter section; and a resistor whose one end is connected to the ground line and whose other end is connected to the input of the second inverter section.

9. The semiconductor integrated circuit device according to Claim 6,

wherein the second gate voltage control circuit comprises: a second inverter section that is connected at its output to the gate of the first PMIS transistor, and has an even number of inverters; a capacitor whose one end is connected to the ground line and whose other end is connected to an input of the second inverter section; and a resistor whose one end is connected to the power supply line and whose other end is connected to the input of the second inverter section.

10. The semiconductor integrated circuit device according to Claim 6,

wherein the second gate voltage control circuit comprises: a second Schmidt trigger circuit connected at its output to the gate of the first PMIS transistor; a capacitor whose one end is connected to the power supply line and whose other end is connected to an input of the second Schmidt trigger circuit; and a resistor whose one end is connected to the ground line and whose other end is connected to the input of the second Schmidt trigger circuit.

11. The semiconductor integrated circuit device according to Claim 1,

wherein the device further comprises an input buffer circuit connected to the external connection terminal.

12. The semiconductor integrated circuit device according to Claim 1,

wherein the device further comprises:

an output circuit connected to the external connection terminal; and

an output prebuffer circuit connected to the output circuit.

13. The semiconductor integrated circuit device according to Claim 12,

wherein the output prebuffer circuit comprises a first prebuffer circuit having at its last stage a first prebuffer connected to the power supply line, and a second prebuffer circuit having at its last stage a second prebuffer connected to the power supply line, and

wherein the output circuit comprises: a second PMIS transistor whose source is connected to the power supply line, whose drain is connected to the external connection terminal, whose gate is connected to an output terminal of the first prebuffer, and whose n-type substrate region is connected to the power supply line; and a second NMIS transistor whose source is connected to the ground line, whose drain is connected to the external connection terminal, whose gate is connected to an output terminal of the second prebuffer, and whose p-type substrate region is connected to the ground line.

14. The semiconductor integrated circuit device according to Claim 1,

wherein the device further comprises an internal circuit connected to the external connection terminal.

15. The semiconductor integrated circuit device according to Claim 1,

wherein the electrostatic discharge protection circuit comprises: a third PMIS transistor whose source is connected to the power supply line, whose drain is connected to the external connection terminal, and whose n-type substrate region is connected to the power supply line; and a third NMIS transistor whose source is connected to the ground line, whose drain is connected to the external connection terminal, and whose p-type substrate region is connected to the ground line.

16. The semiconductor integrated circuit device according to Claim 15,

wherein the device further comprises:

a resistor interposed between the gate of the third PMIS transistor and the power supply line; and

a resistor interposed between the gate of the third NMIS transistor and the ground line.

17. The semiconductor integrated circuit device according to Claim 1,

wherein the electrostatic discharge protection circuit comprises: a first PN diode whose one end is connected to the power supply line and whose other end is connected to the external connection terminal; and a second PN diode whose one end is connected to the ground line and whose other end is connected to the external connection terminal.